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**Abstract of the Disclosure**

5 A processing engine including a processor pipeline 820 with a number  
of pipeline stages, a number of resources and a pipeline protection  
mechanism. The pipeline protection mechanism includes, for each protected  
resource, interlock detection circuitry 1402 for anticipating and/or detecting  
access conflicts for that resource between the pipeline stages. An output of  
the interlock detection circuitry is connected to reservation and filtering  
10 circuitry 1404 for selection of a shadow register. If a shadow register is  
available, shadow management circuitry 1406 generates corresponding  
control signals 1410, 1411 to a set of shadow registers 1400. By writing into  
a selected register, a pipeline conflict is resolved. At a later cycle, a delayed  
write to a corresponding target register restores the pipeline. Conflicts that  
15 cannot be resolved are merged by merge circuitry 1440 to form stall control  
signals for controlling the selective stalling of the pipeline to avoid the  
resource access conflicts. The resources could, for example, be registers in  
register file 832 or parts (fields) within registers. By providing arbitration  
logic within the interlock detection circuitry for each resource, an  
20 embodiment of the invention effectively enables a distribution of the control  
logic needed to anticipate potential resource access conflicts, and allows  
selectively stalling of the pipeline to avoid the conflicts from actually  
occurring.